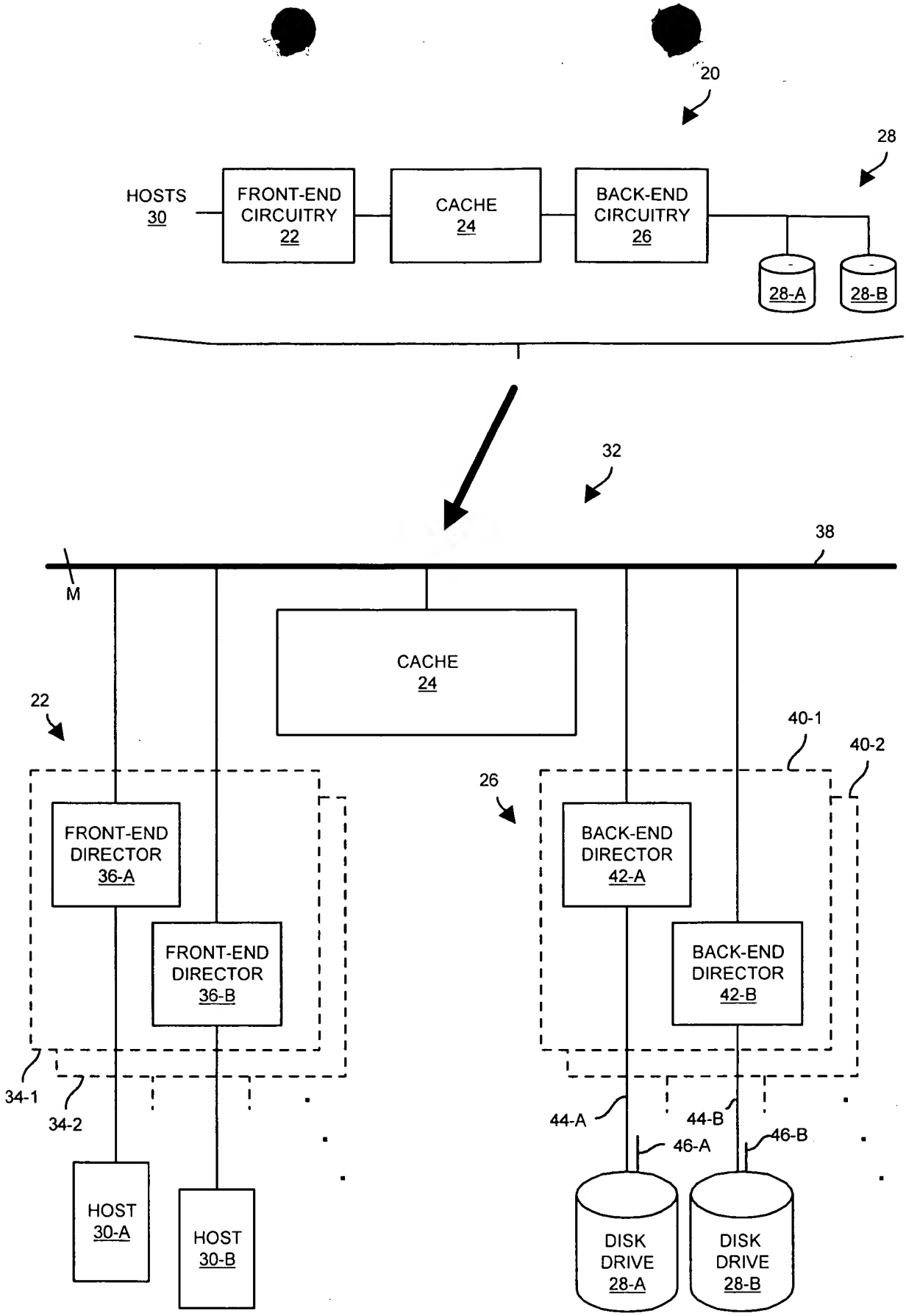


FIG. 1
(PRIOR ART)

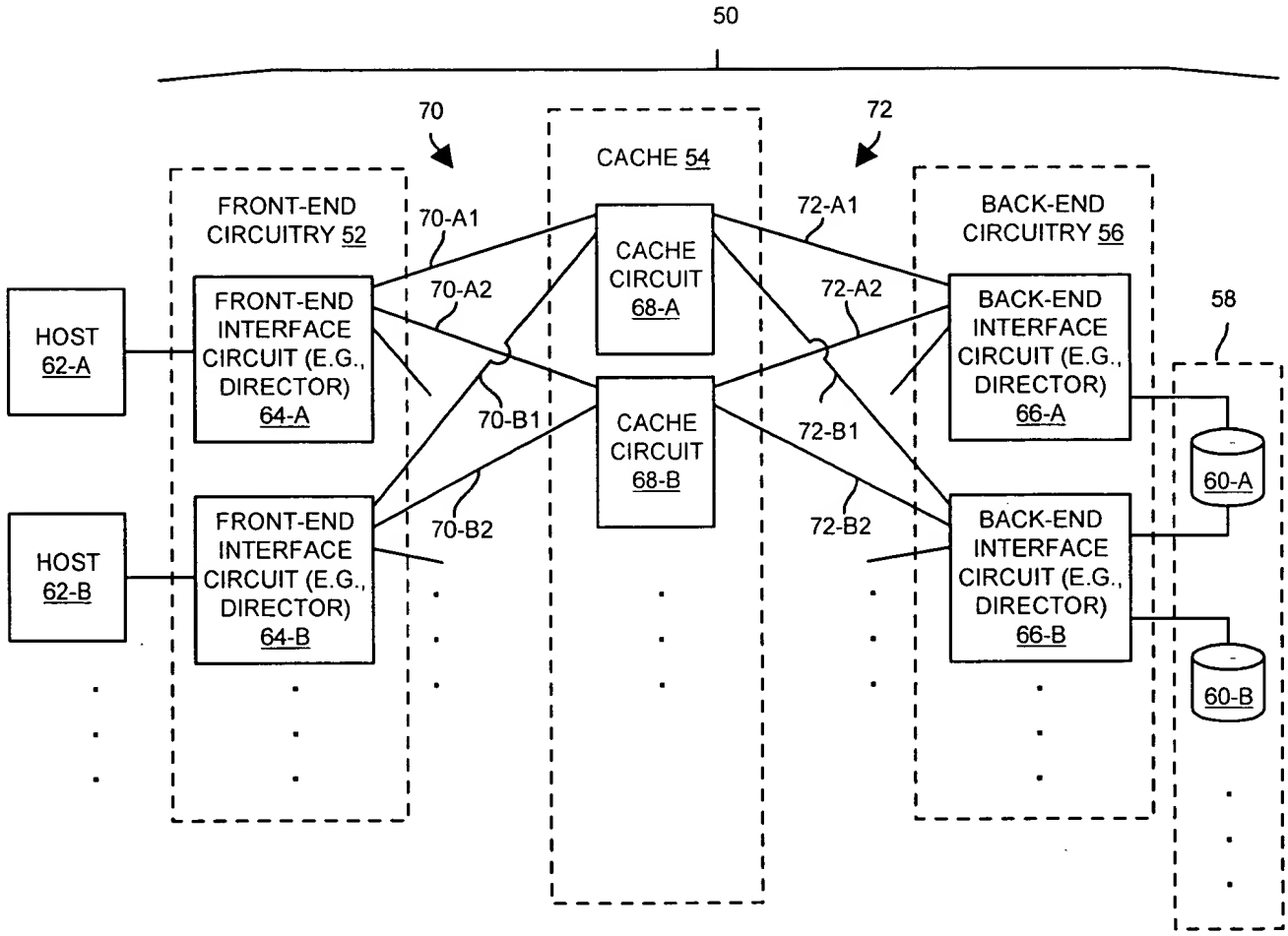

50
70
72
CACHE 54
FRONT-END CIRCUITRY 52
BACK-END CIRCUITRY 56
70-A1
72-A1
CACHE CIRCUIT 68-A
HOST 62-A
FRONT-END INTERFACE CIRCUIT (E.G., DIRECTOR) 64-A
70-A2
72-A2
BACK-END INTERFACE CIRCUIT (E.G., DIRECTOR) 66-A
58
70-B1
72-B1
CACHE CIRCUIT 68-B
60-A
HOST 62-B
FRONT-END INTERFACE CIRCUIT (E.G., DIRECTOR) 64-B
70-B2
72-B2
BACK-END INTERFACE CIRCUIT (E.G., DIRECTOR) 66-B
60-B

FIG. 2

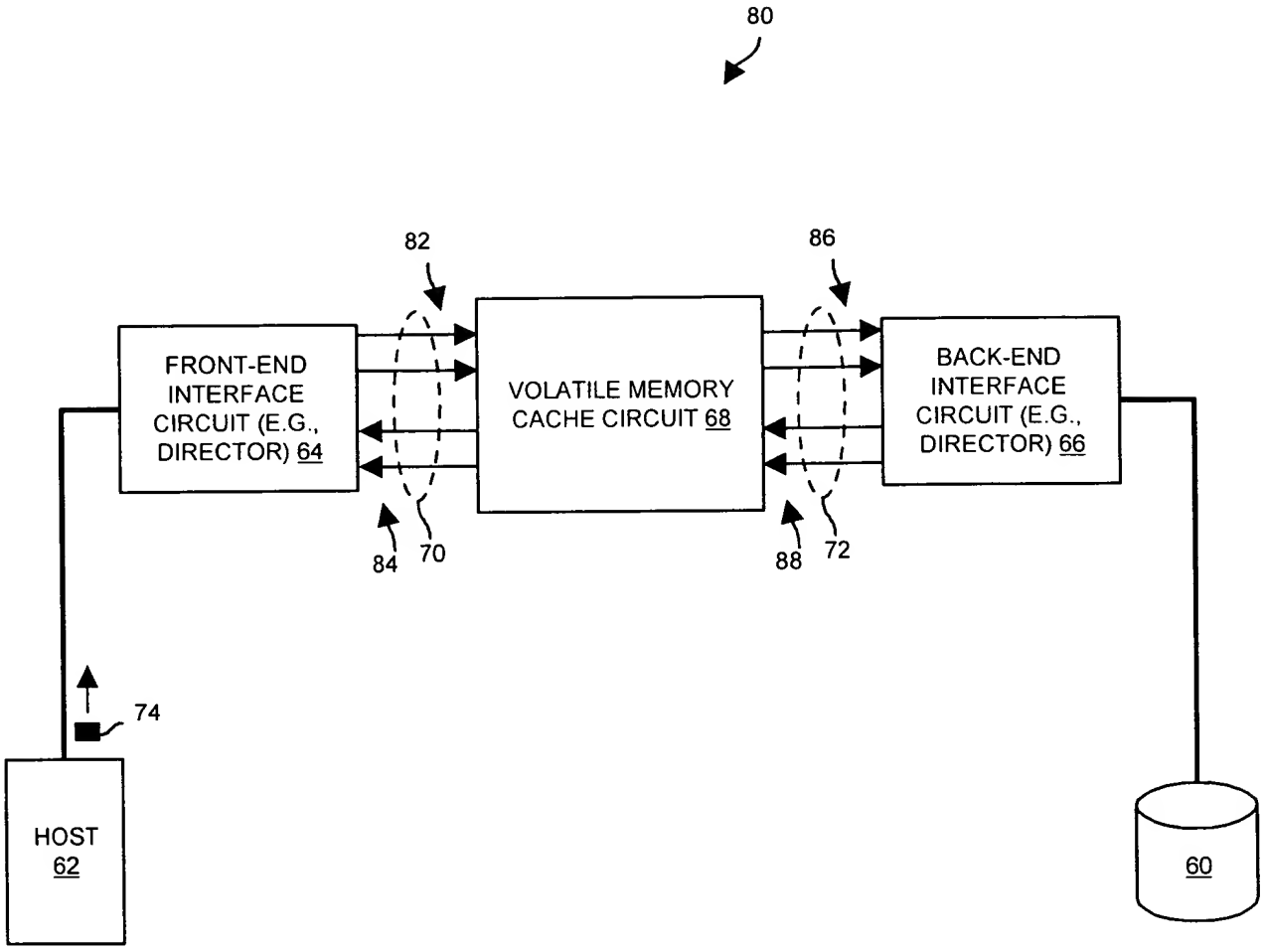

80
82
86
FRONT-END INTERFACE CIRCUIT (E.G., DIRECTOR) 64
VOLATILE MEMORY CACHE CIRCUIT 68
BACK-END INTERFACE CIRCUIT (E.G., DIRECTOR) 66
84
70
88
72
74
HOST 62
60

FIG. 3

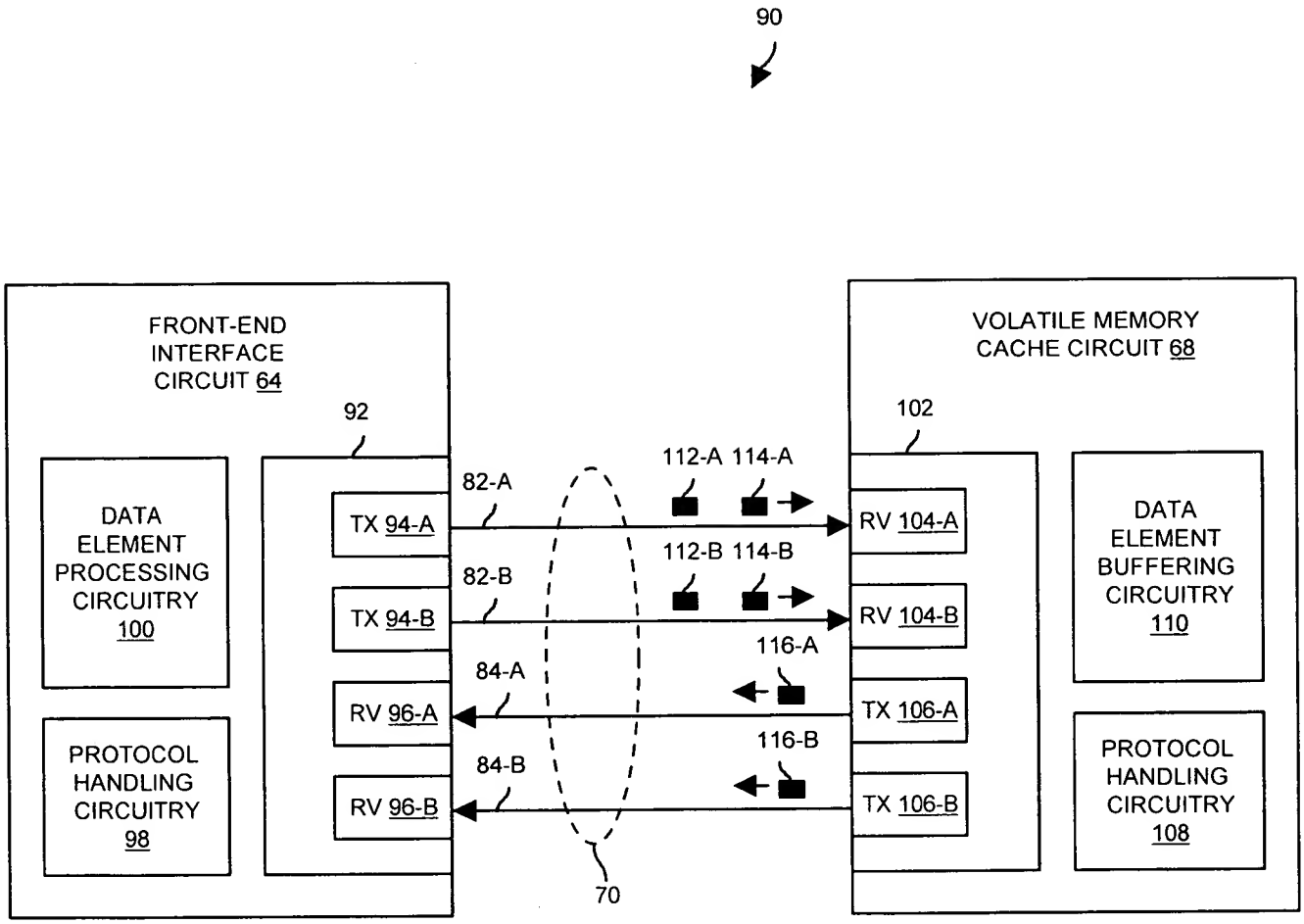

90
FRONT-END INTERFACE CIRCUIT 64
92
DATA ELEMENT PROCESSING CIRCUITRY 100
PROTOCOL HANDLING CIRCUITRY 98
TX 94-A
TX 94-B
RV 96-A
RV 96-B
82-A
82-B
84-A
84-B
112-A
114-A
112-B
114-B
116-A
116-B
70
VOLATILE MEMORY CACHE CIRCUIT 68
102
RV 104-A
RV 104-B
TX 106-A
TX 106-B
DATA ELEMENT BUFFERING CIRCUITRY 110
PROTOCOL HANDLING CIRCUITRY 108

FIG. 4

ACCESS REQUEST FORMAT 140 (E.G., WRITE REQUEST)

SOF 144	COMMAND 146	ADDRESS 148	TAG 150	ERROR DETECTION CODE 152

DATA ELEMENT PORTION FORMAT 142 (E.G., WRITE DATA)

MOF 154	DATA 156	ERROR DETECTION CODE 158	EOF 160

FIG. 5A

STATUS MESSAGE FORMAT 170 (E.G., WRITE ACKNOWLEDGMENT)

MOF 172	TAG 174	FILL 176	STATUS 178	ERROR DETECTION CODE 180	EOF 182

FIG. 5B

ACCESS REQUEST FORMAT 190 (E.G., READ REQUEST)

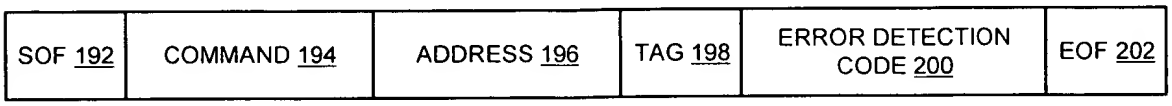
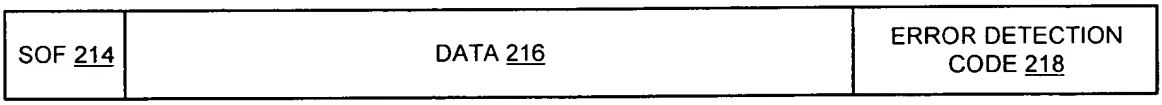


FIG. 6A

DATA ELEMENT PORTION FORMAT 210 (E.G., READ DATA)



STATUS MESSAGE FORMAT 212 (READ ACKNOWLEDGMENT)

FIG. 6B

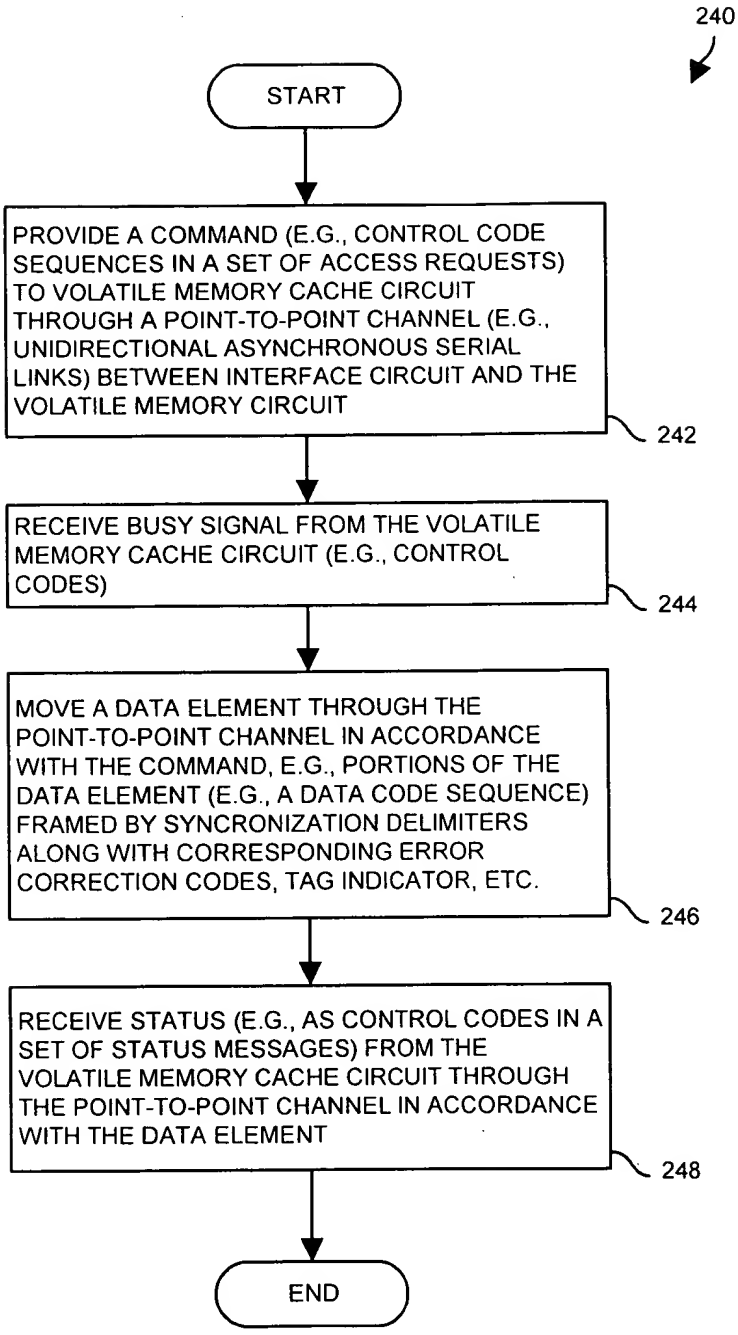

240
START
PROVIDE A COMMAND (E.G., CONTROL CODE SEQUENCES IN A SET OF ACCESS REQUESTS) TO VOLATILE MEMORY CACHE CIRCUIT THROUGH A POINT-TO-POINT CHANNEL (E.G., UNIDIRECTIONAL ASYNCHRONOUS SERIAL LINKS) BETWEEN INTERFACE CIRCUIT AND THE VOLATILE MEMORY CIRCUIT
242
RECEIVE BUSY SIGNAL FROM THE VOLATILE MEMORY CACHE CIRCUIT (E.G., CONTROL CODES)
244
MOVE A DATA ELEMENT THROUGH THE POINT-TO-POINT CHANNEL IN ACCORDANCE WITH THE COMMAND, E.G., PORTIONS OF THE DATA ELEMENT (E.G., A DATA CODE SEQUENCE) FRAMED BY SYNCRONIZATION DELIMITERS ALONG WITH CORRESPONDING ERROR CORRECTION CODES, TAG INDICATOR, ETC.
246
RECEIVE STATUS (E.G., AS CONTROL CODES IN A SET OF STATUS MESSAGES) FROM THE VOLATILE MEMORY CACHE CIRCUIT THROUGH THE POINT-TO-POINT CHANNEL IN ACCORDANCE WITH THE DATA ELEMENT
248
END

FIG. 7

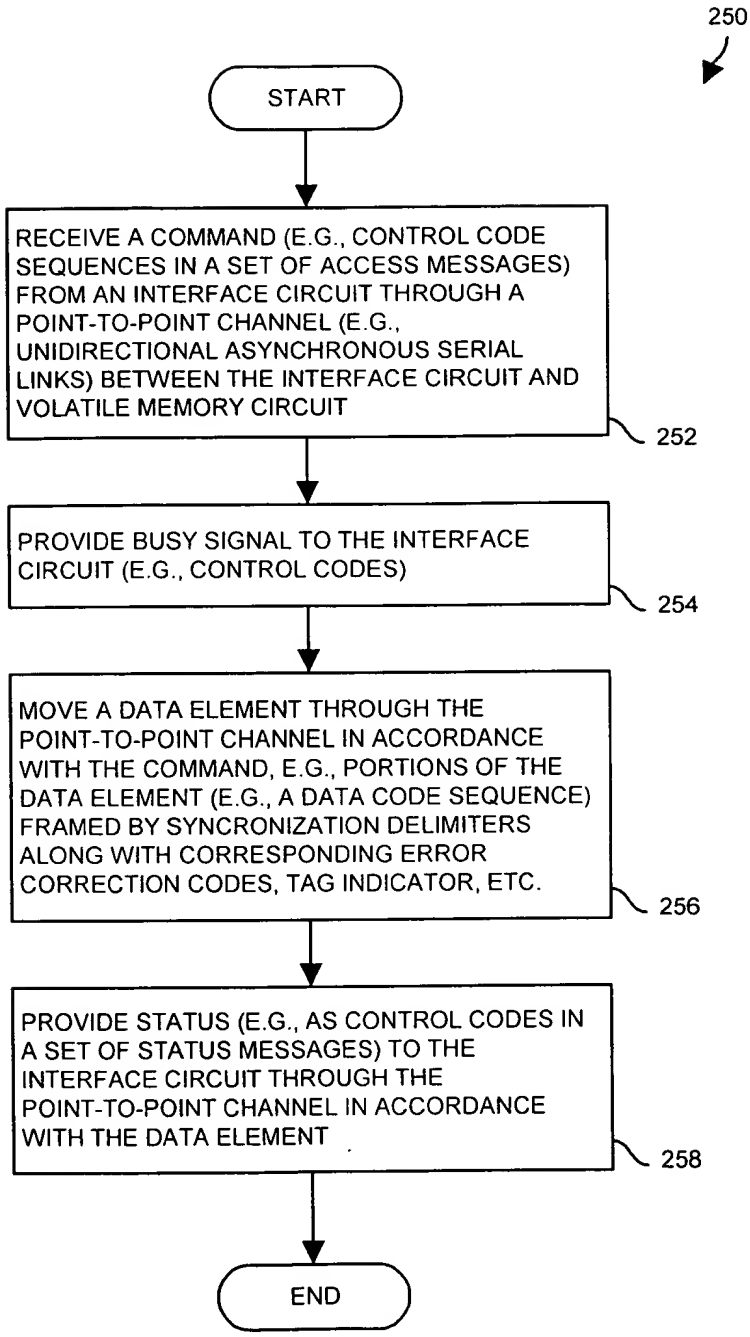

250
START
RECEIVE A COMMAND (E.G., CONTROL CODE SEQUENCES IN A SET OF ACCESS MESSAGES) FROM AN INTERFACE CIRCUIT THROUGH A POINT-TO-POINT CHANNEL (E.G., UNIDIRECTIONAL ASYNCHRONOUS SERIAL LINKS) BETWEEN THE INTERFACE CIRCUIT AND VOLATILE MEMORY CIRCUIT
252
PROVIDE BUSY SIGNAL TO THE INTERFACE CIRCUIT (E.G., CONTROL CODES)
254
MOVE A DATA ELEMENT THROUGH THE POINT-TO-POINT CHANNEL IN ACCORDANCE WITH THE COMMAND, E.G., PORTIONS OF THE DATA ELEMENT (E.G., A DATA CODE SEQUENCE) FRAMED BY SYNCRONIZATION DELIMITERS ALONG WITH CORRESPONDING ERROR CORRECTION CODES, TAG INDICATOR, ETC.
256
PROVIDE STATUS (E.G., AS CONTROL CODES IN A SET OF STATUS MESSAGES) TO THE INTERFACE CIRCUIT THROUGH THE POINT-TO-POINT CHANNEL IN ACCORDANCE WITH THE DATA ELEMENT
258
END

FIG. 8